WHAT IS CLAIMED IS:

1. A system, comprising

a digital section, including

a first driving device having a switch and a logic gate, the first driving device configured to receive a first digital signal and generate a first drive signal therefrom, and

a second driving device having a switch and a logic gate, the second driving device configured to receive a second digital signal and generate a second drive signal therefrom, and

an analog section configured to receive the first and second drive signals and generate first and second respective analog signals therefrom,

wherein rise and fall times of the first and second drive signals are substantially equal.

2. The system of claim 1, wherein the logic gates in the first and second driving devices are NOR gates.

3. The system of claim 2, wherein a first input of each of the NOR gates is coupled to a respective one of the switches and a second input of each of the NOR gates is coupled to an output of an opposite one of the NOR gates.

4. The system of claim 2, wherein the analog device comprises:

a first p-type transistor device receiving the first drive signal to generate the first analog signal therefrom; and

a second p-type transistor receiving the second drive signal to generate the second analog signal therefrom.

5. The system of claim 1, wherein the logic gates in the first and second driving devices are NAND gates.

6. The system of claim 5, wherein a first input of each of the NAND gates is coupled to a respective one of the switches and a second input of each of the NAND gates is coupled to an output of another one of the NAND gates.

7. The system of claim 5, wherein the analog device comprises:

a first n-type transistor device receiving the first drive signal to generate the first analog signal therefrom; and

a second n-type transistor device receiving the second drive signal to generate the second analog signal therefrom.

8. The system of claim 1, wherein the digital section further comprises:

an acceleration system coupled to the first and second driving devices and configured to accelerate the rise and fall times of the first and second drive signals.

9. The system of claim 8, wherein the acceleration system comprises:

a first and second inverters coupled in parallel to each other.

10. The system of claim 9, wherein:

the first inverter is coupled at its input to the first driving device and at its output to the second driving device; and

the second inverter is coupled at its input to the second driving device and at its output to the first driving device.

11. The system of claim 8, wherein the acceleration system is a latch.

12. A system comprising:

a digital section configured to receive digital signals including a means for generating first and second drive signals having substantially equal rise and fall times therefrom; and

an analog section configured to receive the first and second drive signals and generate first and second analog signals therefrom.

13. The system of claim 12, wherein the means for generating comprises first and second logic devices.

14. The system of claim 13, wherein the first and second logic devices are NOR gates.

15. The system of claim 13, wherein the first and second logic devices are NAND gates.

16. The system of claim 12, wherein the digital section further comprises a means for accelerating the rise and fall times of the first and second drive signals.

17. The system of claim 16, wherein the means for accelerating comprises first and second inverters.

18. The system of claim 16, wherein the means for accelerating comprises a latch.